Power Quality Enhancement Using Power Balance Theory Based DSTATCOM

Jampana BANGARRAJU[1], *Veeramalla RAJAGOPAL*[2], *Askani JAYA LAXMI*[3]

[1]Department of Electrical & Electronics Engineering, B. V. Raju Institute of Technology, Narsapur, Medak, Telangana 502 313, India
[2]Department of Electrical & Electronics Engineering, Stanley College of Engineering and Technology for Women, Abids, Hyderabad, Telangana 500001, India
[3]Department of Electrical & Electronics Engineering, College of Engineering Hyderabad, Jawaharlal Nehru Technological University Hyderabad (JNTUH), Kukatpally, Hyderabad, Telangana 500 085, India

rajujbr@gmail.com, rajsarang@gmail.com, ajl1994@yahoo.co.in

DOI: 10.15598/aeee.v14i1.1342

Abstract. *The DSTATCOM (Distributed Static Compensator) is used for current harmonic mitigation, Power Factor Correction (PFC), reactive power compensation, load balancing and neutral current compensation in the Power Distribution System (PDS). In this paper, the power balance theory based DSTATCOM is used for power quality enhancement like current harmonic mitigation, power factor correction (PFC), reactive power compensation, load balancing and neural current compensation and load balancing. A non-isolated star/delta transformer is to reduce dc-link voltage (v_{dc}) of Voltage Source Converter (VSC) and neutral current compensation. The reference source currents can be extracted quickly by using proposed power balance theory. The proposed power balance theory based DSTATCOM is modeled and simulated using MATLAB/SIMULINK under PFC and ZVR (Zero Voltage Regulation) operations.*

Keywords

DSTATCOM, harmonics, power balance theory, power quality, star/delta transformer.

1. Introduction

The power distribution system network is highly polluted due to the presence of power electronic and lagging power factor loads. Because of this, the power quality of supply delivered to the residential, commercial and industrial loads is also much affected [1], [2]. These power electronic based converters create pollution to PDS and also reduce utilization of equipment to their rated value [3]. The major power quality problems are voltage/current harmonics, voltage flicker, transients, sag/swell, load unbalancing, high reactive power, excessive neutral current and poor voltage regulation, etc [4]. A group of power electronic based Custom Power Devices (CPD) such as DSTATCOM, DVR and UPQC are used for mitigation of power quality problems at the three-phase AC source and as well as at load [5]. The power quality at power distribution system is governed by many standards such as IEEE519, IEEE1159, IEEE241, and IEC61642, etc [6].

DSTATCOM is a shunt connected custom power device, which mitigates PQ problems such as power factor correction at the source, current harmonics, reactive power compensation, load unbalancing, etc. The classification of various topologies and control algorithms are reported in the literature [7], [8]. The design, selection of DC bus capacitor, interfacing AC inductor and IGBTs of DSTATCOM are discussed [9]. The primary requirement of any CPD is a quick detection of distortion with high accuracy, a quick response of controller and a generation of reference signals [10], [11]. For a generation of reference signals, many control algorithms are reported in the literature such as sinusoid-tracking algorithm [12], SRF theory based control algorithm [13], parallel neural network based algorithm [14] and nonlinear control algorithm [15].

In this paper, power balance theory based DSTATCOM for power factor correction and zero voltage regulation mode operations of DSTATCOM for mitigation of current related PQ problems such as excessive reactive power component, currents harmonics, power factor correction and unbalanced loads have

been presented [16]. A three-phase star/delta transformer is connected at the Point of Common Coupling (PCC) to compensate neutral current and also reduces DC link voltage of capacitor [17], [18].

The features of proposed DSTATCOM are:

- Power Factor Correction (PFC) operation: harmonics compensation, unity power factor maintenance at source and load balancing.
- Zero Voltage Regulation (ZVR) operation: harmonics compensation, unity power factor maintenance at the source, reactive power compensation, and load balancing.
- Control strategy is robust, simple and efficient.
- Star/delta transformer is used to reduce the DC-link voltage of VSC and for neutral current compensation.

The performance of power balance theory based DSTATCOM is modeled and simulated using MATLAB/SIMULINK with linear/non-linear R-L loads under PFC and ZVR operations.

2. Design and Characteristics of DSTATCOM

The schematic diagram of power balance theory based DSTATCOM with star/delta transformer in a distri-

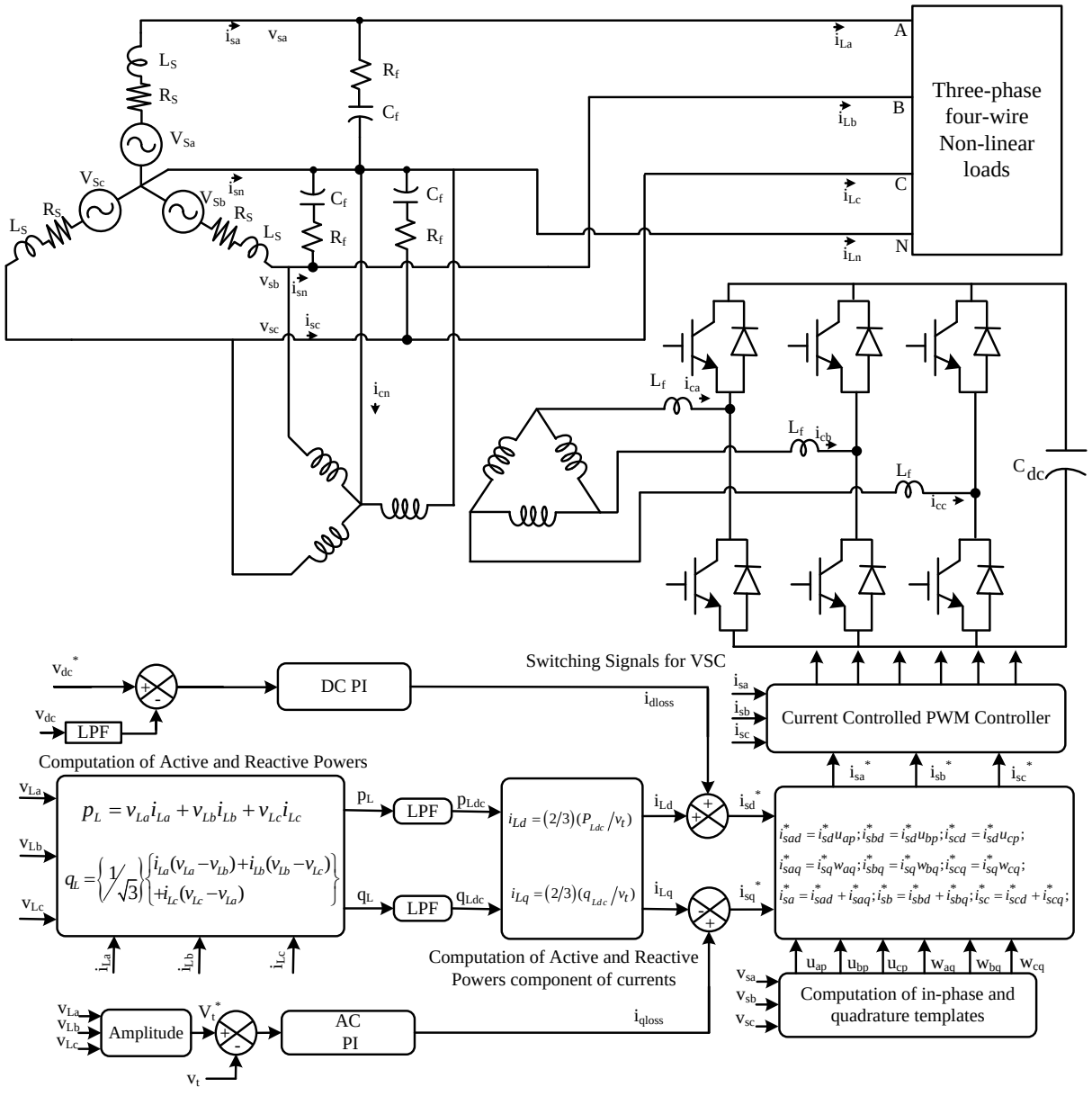


Fig. 1: Schematic diagram of power balance theory for DSTATCOM with star/delta transformer.

bution system is shown in Fig. 1. The proposed DSTATCOM consists of a three-leg VSC (Voltage Source Converter), a DC bus capacitor (C_{dc}) and three single-phase AC inductors (L_f). The VSC consists of six IGBT switches with anti-parallel diodes, and AC inductor (L_f) is used to mitigate ripples in the compensated currents. The three-phase supply voltages (v_{sa}, v_{sb}, v_{sc}) with source impedance Z_s (R_s and L_s) and three-phase loads may be linear/nonlinear R-L loads. A Ripple filter consists of resistance (R_f) and capacitance (C_f) connected across PCC (Point of Common Coupling) to compensate high frequency voltage harmonics. The proposed DSTATCOM injects compensating currents (i_{ca}, i_{cb}, i_{cc}) to cancel the reactive power component of load currents and harmonics of the non-linear loads.

3. Proposed Power Balance Theory for DSTATCOM

Figure 1 shows the proposed power balance theory based DSTATCOM in the three-phase distribution system. The main advantage of power balance theory is the fast detection of distortion with high accuracy and quick response extraction of reference source currents. The star/delta transformer is connected at PCC to compensate neural current and to reduce DC link voltage. The basic equations of power balance theory for generation of switching signals for VSC are given below.

3.1. In-Phase Component of Reference Source Currents

The in-phase unit vectors for reference source currents are estimated as:

$$v_t = \left(\frac{2}{3}\right)^{1/2} \cdot \left(V_{sa}^2 + v_{sb}^2 + v_{sc}^2\right)^{1/2}, \tag{1}$$

where v_t is the amplitude of the terminal voltage at PCC.

$$\begin{aligned} u_{ap} &= v_{sa}/v_t, \\ u_{bp} &= v_{sb}/v_t, \\ u_{cp} &= v_{sc}/v_t. \end{aligned} \tag{2}$$

The instantaneous active load power (p_L) are estimated as:

$$p_L = v_{La}i_{La} + v_{Lb}i_{Lb} + v_{Lc}i_{Lc}. \tag{3}$$

This instantaneous active load power (p_L) consists of AC and DC components. An LPF (Low Pass Filter) is used to extract DC component of load power (P_{Ldc}). The magnitude of the fundamental active power component of load current can be estimated as:

$$i_{Ld} = (2/3)(P_{Ldc}/v_t). \tag{4}$$

The DC bus voltage error of VSC ($v_{erdc(m)}$) at m$^{\text{th}}$ sample instant is given by:

$$v_{erdc(m)} = v^*_{dc(m)} - v_{dc(m)}, \tag{5}$$

where $v^*_{dc(m)}$ is the reference DC bus voltage, and $v_{dc(m)}$ is the sensed DC bus voltage of VSC at m$^{\text{th}}$ sample instant. The output of the DC PI controller is to control DC bus voltage of the VSC at mth sample instant, which is given by:

$$\begin{aligned} i_{dloss(m)} = i_{dloss(m-1)} &+ k_{dp}\{v_{erdc(m)} - v_{erdc(m-1)}\} \\ &+ k_{di}\{v_{erdc(m)}\}, \end{aligned} \tag{6}$$

where $i_{dloss(m)}$ is current loss component of DC bus voltage controller. The k_{dp} and k_{di} are the proportional and integral gains of the DC bus PI controller. This loss component current (i_{dloss}) is added to the magnitude of the fundamental active power component of load current (i_{Ld}):

$$i^*_{sd} = i_{dloss} + i_{Ld}, \tag{7}$$

where i^*_{sd} is considered as the magnitude of in-phase reference source current of the VSC. The in-phase component of reference source currents (i^*_{sad}, i^*_{nsbd}, i^*_{scd}) are given below:

$$\begin{aligned} i^*_{sad} &= i^*_{sd}u_{ap}, \\ i^*_{sbd} &= i^*_{sd}u_{bp}, \\ i^*_{scd} &= i^*_{sd}u_{cp}. \end{aligned} \tag{8}$$

3.2. Quadrature Component of Reference Source Currents

The quadrature vector for reference source currents are estimated as:

$$w_{aq} = -\frac{u_{bp}}{\sqrt{3}} + \frac{u_{cp}}{\sqrt{3}}, \tag{9}$$

$$w_{bq} = \frac{\sqrt{3}u_{ap}}{2} + \frac{u_{bp} - u_{cp}}{2}\sqrt{3}, \tag{10}$$

$$w_{cq} = -\frac{\sqrt{3}u_{ap}}{2} + \frac{u_{bp} - u_{cp}}{2}\sqrt{3}. \tag{11}$$

The instantaneous reactive load power (q_L) are estimated as:

$$\begin{aligned} q_L = \frac{1}{\sqrt{3}}\{&i_{La}(v_{La} - v_{Lb}) + i_{Lb}(v_{Lb} - v_{Lc}) \\ &+ i_{Lc}(v_{Lc} - v_{La})\}. \end{aligned} \tag{12}$$

This instantaneous reactive load power (q_L) consists of AC and DC components. An LPF is used to extract

DC component of load power (q_{Ldc}). The magnitude of the fundamental reactive power component of load current can be estimated as:

$$i_{Lq} = \frac{2}{3}\frac{q_{Ldc}}{v_t}. \tag{13}$$

The terminal voltage error at PCC ($v_{ert(m)}$) at m$^{\text{th}}$ sample instant is given by:

$$v_{ert(m)} = v^*_{t(m)} - v_{t(m)}, \tag{14}$$

where $v^*_{t(m)}$ is the reference terminal voltage at PCC and $v_{t(m)}$ is the sensed terminal voltage at PCC at m$^{\text{th}}$ sample instant. The output of the AC bus PI controller is to control terminal voltage at m$^{\text{th}}$ sample instant, which is given as:

$$\begin{aligned} i_{qloss(m)} = i_{qloss(m-1)} + k_{qp}\{v_{ert(m)} - v_{ert(m-1)}\} \\ +k_{qi}\{v_{ert(m)}\}, \end{aligned} \tag{15}$$

where $i_{qloss(m)}$ is current loss component of AC bus voltage controller. The k_{qp} and k_{qi} are the proportional and integral gains of the AC bus PI controller. This loss component current (i_{qloss}) is added to the magnitude of the fundamental reactive power component of load current (i_{Lq}):

$$i^*_{sq} = i_{qloss} + i_{sq}, \tag{16}$$

where i^*_{sq} is considered as the magnitude of quadrature reference source current. The quadrature phase component of reference source currents (i^*_{saq}, i^*_{sbq}, i^*_{scq}) are given below:

$$\begin{aligned} i^*_{saq} &= i^*_{sq} w_{aq}, \\ i^*_{sbq} &= i^*_{sq} w_{bq}, \\ i^*_{scq} &= i^*_{sq} w_{cq}. \end{aligned} \tag{17}$$

3.3. Generation of Reference Source Currents for VSC

The generations of reference source currents for three-leg VSC are summation of in-phase and quadrature phase component of reference source current:

$$\begin{aligned} i^*_{sa} &= i^*_{sad} + i^*_{saq}, \\ i^*_{sb} &= i^*_{sbd} + i^*_{sbq}, \\ i^*_{sc} &= i^*_{scd} + i^*_{scq}. \end{aligned} \tag{18}$$

3.4. Star/Delta Transformer Connection

The three-phase star/delta transformer is used for neural current compensation and also reduces DC link voltage of VSC. The star/delta transformer connection is depicted in Fig. 2. The primary winding voltage per phase is:

$$v_{An} = \frac{v_{LL}}{\sqrt{3}} = \frac{415}{\sqrt{3}} = 239.6 \text{ V}. \tag{19}$$

Hence, star/delta transformer rated voltage is selected as 240 V. The secondary voltage of delta winding is also selected as 240 V. The rating of three single-phase transformers is 3 kVA, 240/240 V.

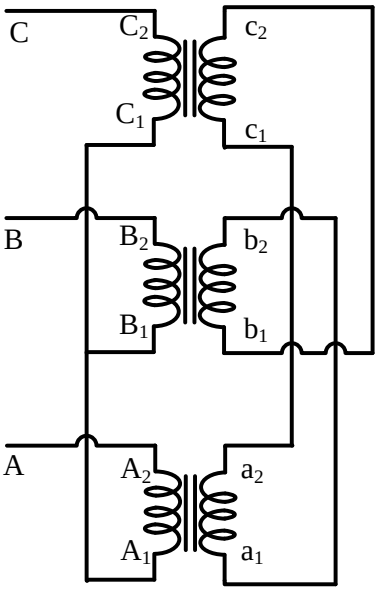


Fig. 2: Star/Delta Transformer connection.

3.5. Current Controlled PWM Controller

The three-phase source current errors (i_{sae}, i_{sbe}, i_{sce}) are the difference between reference source currents (i^*_{sa}, i^*_{sb}, i^*_{sc}) and source currents (i_{sa}, i_{sb}, i_{sc}). These source current errors are compared with triangular wave frequency (f_s) of 10 kHz for generating of switching signals for three-leg VSC.

4. Results and Discussion

The proposed power balance theory based DSTATCOM is modeled and simulated by using MATLAB/SIMULINK. The performance of the power balance theory for DSTATCOM is studied for PFC and ZVR modes of operation under linear/nonlinear R-L loads and results are discussed in the following sections.

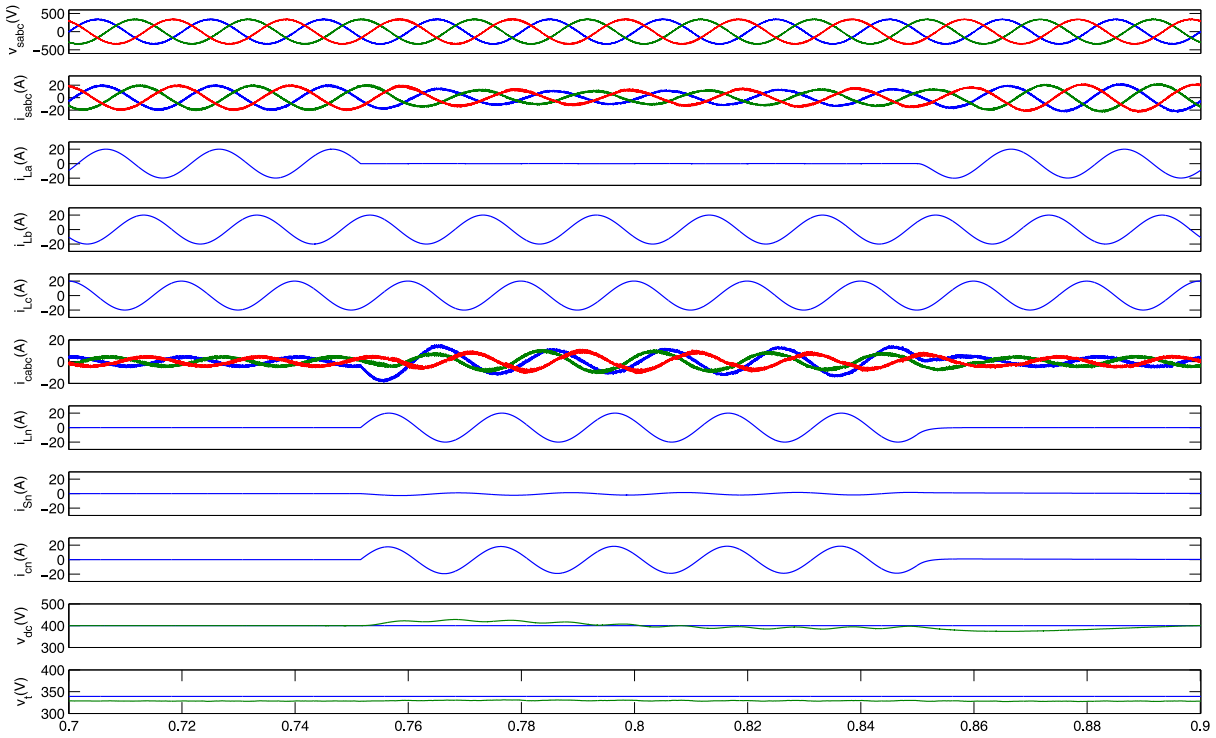


Fig. 3: Performance of DSTATCOM with linear loads under PFC mode.

4.1. Performance of Power Balance Theory Based DSTATCOM Under PFC Mode with Linear Loads

The performance of power balance theory based DSTATCOM under PFC mode with linear loads is shown in Fig. 3. The proposed DSTATCOM parameters such as source voltage (v_{sabc}), source current (i_{sabc}), load phase currents (i_{La}, i_{Lb}, i_{Lc}), compensating current (i_{cabc}), load neutral current (i_{Ln}), source neutral current (i_{sn}), compensating neutral current (i_{cn}), DC bus voltage (v_{dc}), its corresponding reference DC bus voltage (v^*_{dc}), terminal voltage (v_t) and its corresponding reference terminal voltage (v^*_t) are shown in Fig. 3. At $t = 0.75$ second, suddenly one phase of the three-phase load was disconnected and after five cycles, it was reapplied again. With different variations in the three-phase linear load, it was observed that the source voltage (v_{sabc}) and source current (i_{sabc}) are in-phase. These variations in three-phase linear load, the performance characteristics of DSTATCOM show that the source voltages (v_{sabc}) and source currents (i_{sabc}) are balanced and harmonic free. The star/delta transformer is used to compensate the load neutral current under unbalanced load condition, during this period source neutral current (i_{sn}) is maintained at zero. The performance parameters shown in Fig. 3 depict DC bus voltage (v_{dc}) and terminal voltage (v_t), which are maintained at 400 V and 320 V respectively.

4.2. Performance of Power Balance Theory Based DSTATCOM Under PFC Mode with Non-Linear Loads

The performance of power balance theory based DSTATCOM under PFC mode with non-linear loads is shown in Fig. 4. The proposed DSTATCOM parameters such as source voltage (v_{sabc}), source current (i_{sabc}), load phase currents (i_{La}, i_{Lb}, i_{Lc}), compensating current (i_{cabc}), load neutral current (i_{Ln}), source neutral current (i_{sn}), compensating neutral current (i_{cn}), DC bus voltage (v_{dc}), its corresponding reference DC bus voltage (v^*_{dc}), terminal voltage (v_t) and its corresponding reference terminal voltage (v^*_t) are shown in Fig. 4. At $t = 0.75$ second, suddenly one phase of the three-phase load is disconnected and after five cycles again it was reapplied. At different variations in the three-phase non-linear load, it was observed that the source voltage (v_{sabc}) and source current (i_{sabc}) are in-phase. These variations in three-phase non-linear load, the performance characteristics of DSTATCOM show that the source voltages (v_{sabc}) and source currents (i_{sabc}) are balanced and harmonic free. The star/delta transformer is used to compensate the load neutral current under unbalanced load condition. During this period source neutral current (i_{sn}) is maintained at zero. The performance parameters shown in Fig. 4 depict DC bus voltage (v_{dc}) and terminal voltage (v_t) which are maintained at 400 V and

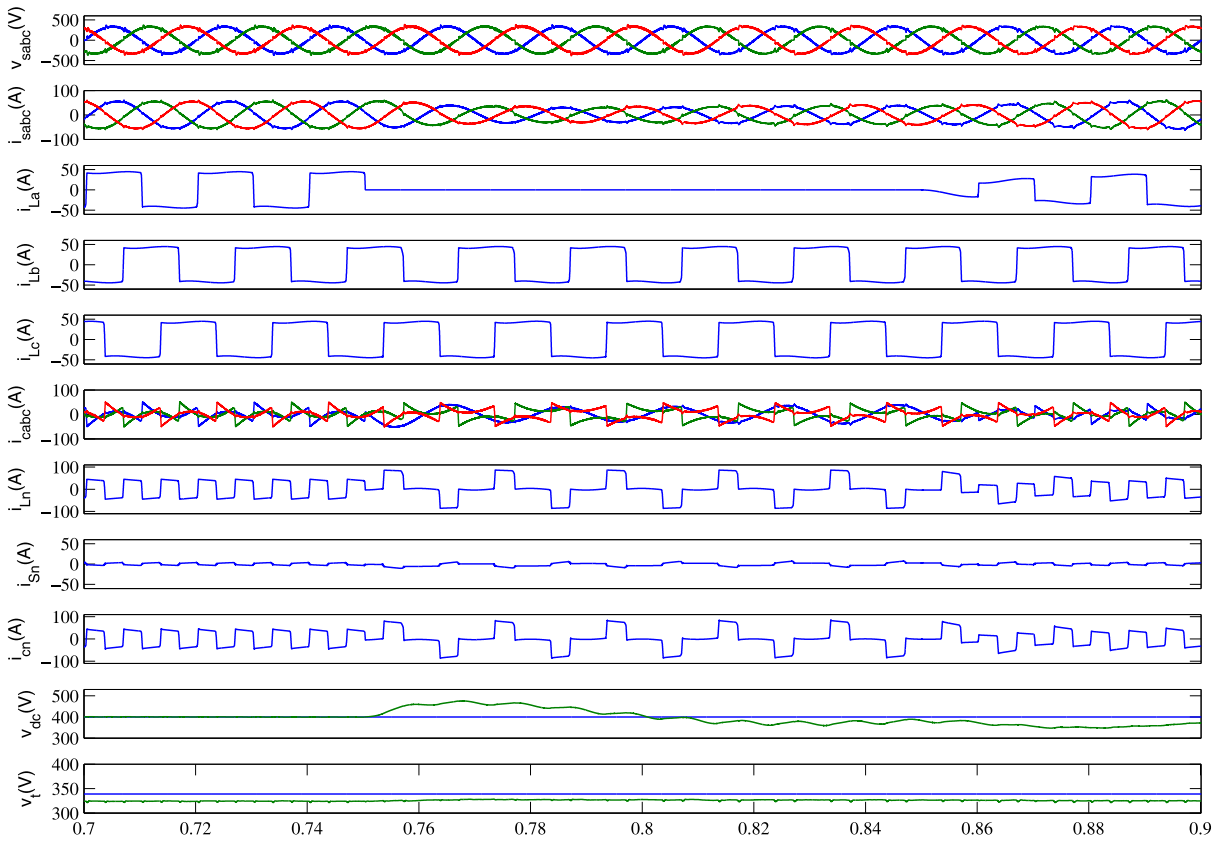


Fig. 4: Performance of DSTATCOM with non-linear loads under PFC mode.

320 V respectively. The source voltage and source current THD are 4.47 % and 3.23 % whereas load current THD is 46.35 % for three-phase non-Linear R-L loads.

4.3. Performance of Power Balance Theory Based DSTATCOM Under ZVR Mode with Linear Loads

The performance of power balance theory based DSTATCOM under ZVR mode with linear loads is shown in Fig. 5. The proposed DSTATCOM parameters such as source voltage (v_{sabc}), source current (i_{sabc}), load phase currents (i_{La}, i_{Lb}, i_{Lc}), compensating current (i_{cabc}), load neutral current (i_{Ln}), source neutral current (i_{sn}), compensating neutral current (i_{cn}), DC bus voltage (v_{dc}), its corresponding reference DC bus voltage (v_{dc}^{*}), terminal voltage (v_t) and its corresponding reference terminal voltage (v_t^{*}) are shown in Fig. 5. At $t = 0.75$ second, suddenly one phase of the three-phase load is disconnected and after five cycles again it was reapplied. At different variations in the three-phase linear load, it was observed that the source voltage (v_{sabc}) and source current (i_{sabc}) are in-phase. These variations in three-phase linear load, the performance characteristics of DSTATCOM show that the source voltages (v_{sabc}) and source currents (i_{sabc}) are balanced and harmonic free. The star/delta transformer is used to compensate load neutral current under unbalanced load condition - during this period source neutral current (i_{sn}) is maintained at zero. The performance parameters shown in Fig. 5 depict DC bus voltage (v_{dc}) and terminal voltage (v_t), which are maintained at 400 V and 339 V respectively.

4.4. Performance of Power Balance Theory Based DSTATCOM Under ZVR Mode with Non-Linear Loads

The performance of power balance theory based DSTATCOM under ZVR mode with non-linear loads is shown in Fig. 6. The proposed DSTATCOM parameters such as source voltage (v_{sabc}), source current (i_{sabc}), load phase currents (i_{La}, i_{Lb}, i_{Lc}), compensating current (i_{cabc}), load neutral current (i_{Ln}), source neutral current (i_{sn}), compensating neutral current (i_{cn}), DC bus voltage (v_{dc}), its corresponding reference DC bus voltage (v_{dc}^{*}), terminal voltage (v_t) and its corresponding reference terminal voltage (v_t^{*}) are shown in Fig. 6. At $t = 0.75$ second, suddenly one phase of the three-phase load is disconnected and after

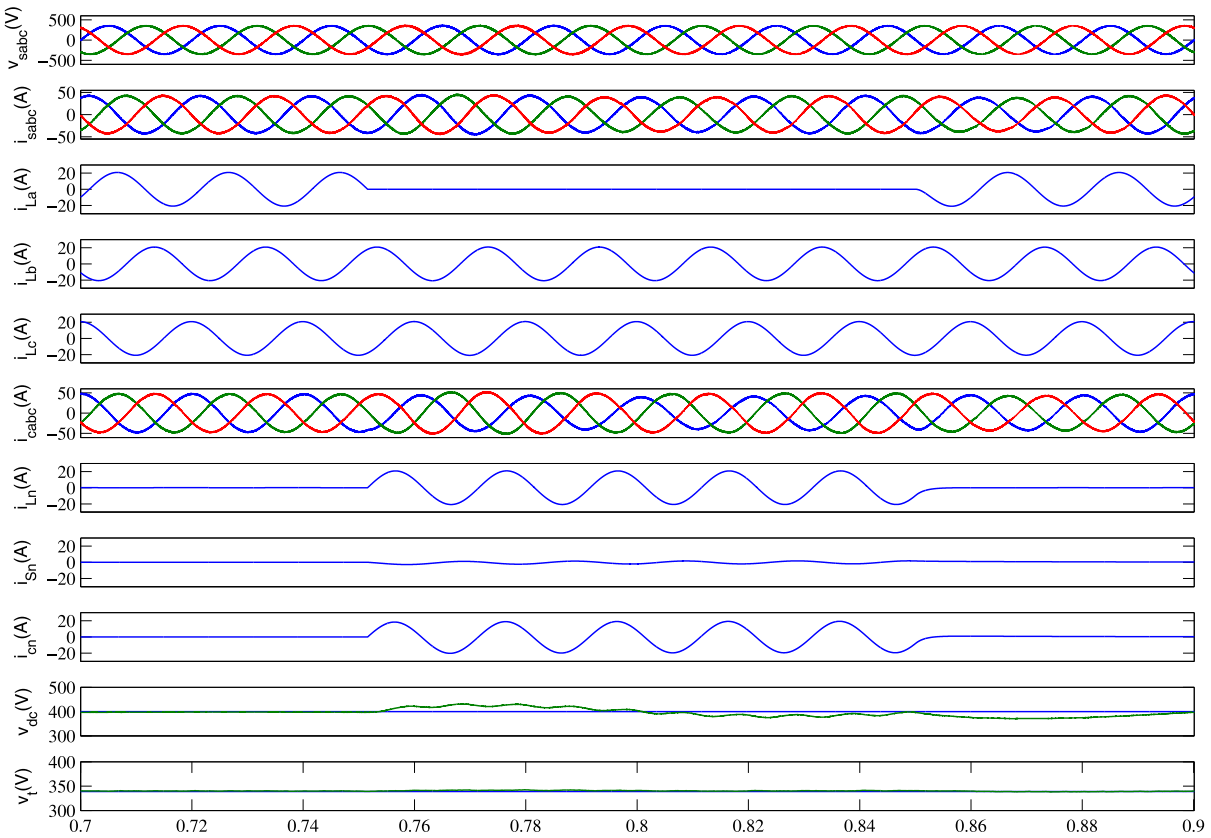


Fig. 5: Performance of DSTATCOM with linear loads under ZVR mode.

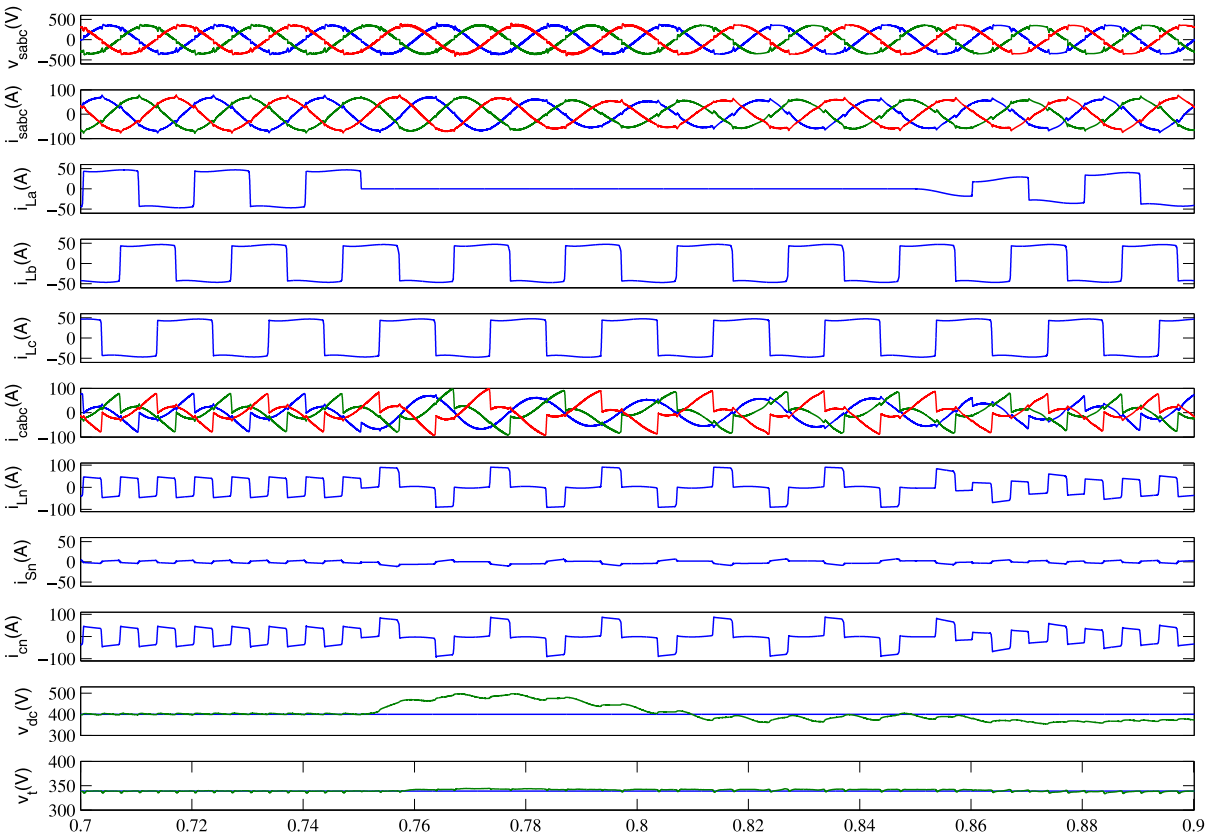
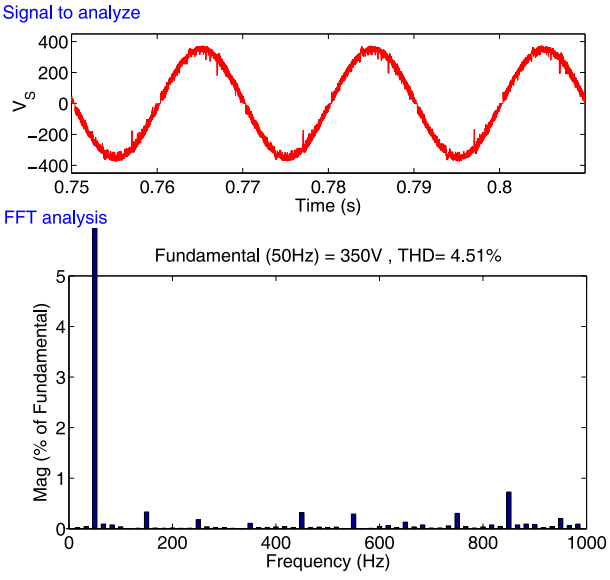
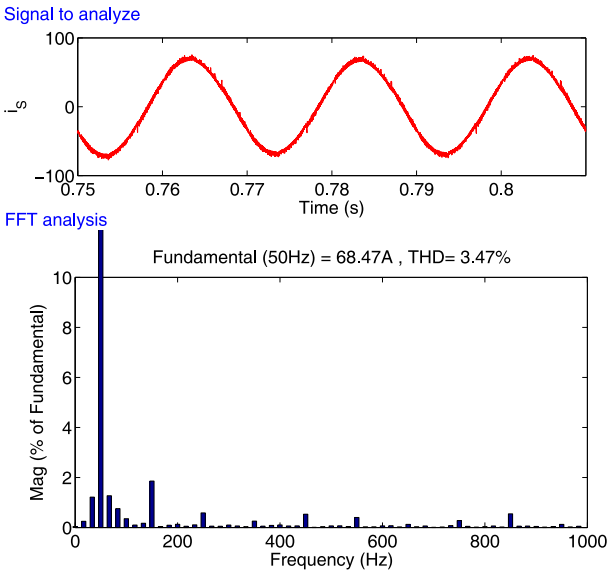


Fig. 6: Performance of DSTATCOM with non-linear loads under ZVR mode.

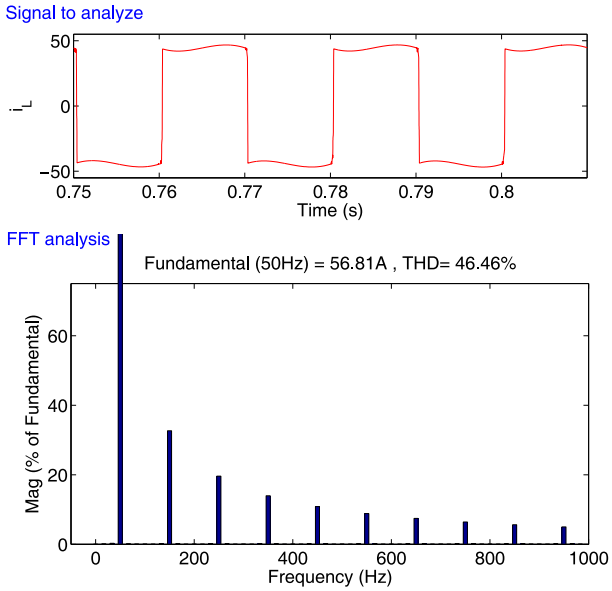
five cycles again it was reapplied. At different variations in the three-phase non-linear load, it was observed that the source voltage (v_{sabc}) and source current (i_{sabc}) are in-phase. These variations in three-phase non-linear load, the performance characteristics of DSTATCOM show that the source voltages (v_{sabc}) and source currents (i_{sabc}) are balanced and harmonic free. The star/delta transformer is used to compensate load neutral current under unbalanced load condition, during this period source neutral current (i_{sn}) is maintained at zero. The performance parameters shown in Fig. 6 depict DC bus voltage (v_{dc}) and terminal voltage (v_t), which are maintained at 400 V and 339 V respectively. The source voltage (v_s) and source current (i_s) THD are 4.51 % and 3.47 % whereas load current (i_L) THD is 46.46 % for three-phase non-linear R-L loads with harmonic spectra as depicted in Fig. 7.



(a) source voltage



(b) source current



(c) load current

Fig. 7: Harmonic spectra.

5. Conclusion

The dynamic performance of power balanced theory based DSTATCOM shows satisfactory results under the application of linear/non-linear R-L loads. The advantage of using star/delta transformer is to mitigate neutral load current and also to reduce the DC link voltage at 400 V. The performance characteristics show that power balance theory based DSTATCOM compensates power quality problems like mitigation of harmonics, power factor correction at the source, load balancing, and reactive power compensation. The power balance theory based DSTATCOM is simple, efficient, reliable and robust as observed from the satisfactory results. During PFC and ZVR operations of DSTATCOM, it maintained the terminal voltage (v_t) and DC bus voltage (v_{dc}) at 339 V and 400 V respectively. The proposed DSTATCOM with non-linear loads reduces the THD of the source voltage (v_s) and source current (i_s) to 4.51 % and 3.47 % respectively, which is well within IEEE519, IEEE1159, IEEE241 and IEC61642 standards.

References

[1] SHORT, T. *Distribution reliability and power quality*. Boca Raton: CRC Press, 2006. ISBN 08-493-9575-5.

[2] GHOSH, A. and G. LEDWICH. *Power quality enhancement using custom power devices*. Boston:

Kluwer Academic Publishers, 2002. ISBN 14-020-7180-9.

[3] DUGAN, R. C., M. MCGRANAGHAN and H. BEATY. *Electrical power systems quality*. 2nd ed. New York: McGraw Hill, 2006. ISBN 00-701-8031-8.

[4] CHAN, M.-Y., K. K. F. LEE and M. W. K. FUNG. A case study survey of harmonic currents generated from a computer centre in an office building. *Journal of Architectural Science Review*. 2011, vol. 50, iss. 3, pp. 274–280. ISSN 0003-8628. DOI: 10.3763/asre.2007.5033.

[5] EMIN MERAL, M., A. TEKE and M. TUMAY. Overview of an extended custom power park. In: *IEEE 2nd International Conference on Power and Energy*. Johor Bahru: IEEE, 2008, pp. 1364–1368. ISBN 978-1-4244-2405-4. DOI: 10.1109/PECON.2008.4762690.

[6] CHATTOPADHYAY, S., M. MITRA and S. SENGUPTA. *Electric Power Quality*. New York: Springer Verlag, 2011. ISBN 94-007-0634-0.

[7] SINGH, B., K. AL-HADDAD and C. AMBRISH. A Review of Acive filters for Power Quality Improvement. *IEEE Transactions Industrial Electronics*. 1999, vol. 46, iss. 5, pp. 960–971. ISSN 0278-0046. DOI: 10.1109/41.793345.

[8] WANG, Y. F. and Y. W. LI. A grid fundamental and harmonic components detection method for single-phase systems. *IEEE Transactions on Power Electronics*. 2013, vol. 28, iss. 5, pp. 2204–2213. ISSN 0885-8993. DOI: 10.1109/TPEL.2012.2214445.

[9] SINGH, B., P. JAYAPRAKASH and D. P. KOTHARI. A T-Connected Transformer and Three leg VSC based DSTATCOM for Power Quality Improvement. *IEEE Transactions on Power Electronics*. 2008, vol. 23, iss. 6, pp. 2710–2718. ISSN 0885-8993. DOI: 10.1109/TPEL.2008.2004273.

[10] NEVES, F. A. S., H. E. P. DE SOUZA, M. C. CAVALCANTI, F. BRADASCHIA and E. J. BUENO. Digital filters for fast harmonic sequence components separation of unbalanced and distorted three-phase signal. *IEEE Transactions on Industrial Electronics*. 2012, vol. 59, iss. 10, pp. 3847–3859. ISSN 0278-0046. DOI: 10.1109/TIE.2011.2163284.

[11] MARIUN, N., A. ALAM, S. MAHMOD and H. HIZAM. Review of control strategies for power quality conditioners. In: *Proceedings of National Power and Energy Conference*. Kuala Lumpur: IEEE, 2004, pp. 109–115. ISBN 0-7803-8724-4. DOI: 10.1109/PECON.2004.1461626.

[12] RAHMANI, S., N. MENDALEK and K. AL-HADDAD. Experimental design of a nonlinear control technique for three-phase shunt active power filter. *IEEE Transactions on Industrial Electronics*. 2010, vol. 57, iss. 10, pp. 3364–3375. ISSN 0278-0046. DOI: 10.1109/TIE.2009.2038945.

[13] SINGH, B. N., B. SINGH, A. CHANDRA and K. AL-HADDAD. Design and digital implementation of active power filters with power balance theory. *IEE Proceedings of Electrical Power Applications*. 2005, vol. 152, iss. 5, pp. 1149–1160. ISSN 1350-2352. DOI: 10.1049/ip-epa:20050097.

[14] ENJETI, P. N., W. SHIREEN, P. PACKEBUSH and I. J. PITEL. Analysis and design of a new active power filter to cancel neutral current harmonics in three phase four-wire electric distribution systems. *IEEE Transactions on Industry Applications*. 1994, vol. 30, iss. 6, pp. 1565–1572. ISSN 0093-9994. DOI: 10.1109/TIA.1994.350311.

[15] JACOBS, J., D. DETJEN, C.-U. KARIPIDIS and R. W. DE DONCKER. Rapid prototyping tools for power electronic systems: demonstration with shunt active power filters. *IEEE Transactions on Power Electronics*. 2004, vol. 19, iss. 2, pp. 500–507. ISSN 0885-8993. DOI: 10.1109/TPEL.2003.823240.

[16] SINGH, B., P. JAYAPRAKASH, T. R. SOMAYAJULU and D. P. KOTHARI. Reduced Rating VSC With a Zig-Zag Transformer for Current Compensation in a Three-Phase Four-Wire Distribution System. *IEEE Transactions on Power Delivery*. 2009, vol. 24, iss. 1, pp. 249–259. ISSN 0885-8977. DOI: 10.1109/TPWRD.2008.2005398.

[17] MONTERO, M. I. M., E. R. CADAVAL and F. B. GONZALEZ. Comparison of control strategies for shunt active power filters in three-phase four-wire systems. *IEEE Transactions on Power Electronics*. 2007, vol. 22, iss. 1, pp. 229–236. ISSN 0885-8993. DOI: 10.1109/TPEL.2006.886616.

[18] SINGH, B. and J. SOLANKI. A comparison of control algorithms for DSTATCOM. *IEEE Transactions on Industrial Electronics*. 2009, vol. 56, iss. 7, pp. 2738–2745. ISSN 0278-0046. DOI: 10.1109/TIE.2009.2021596.

About Authors

Jampana BANGARRAJU was born in Tanuku, India, in 1982. He received the B.Sc. degree in

Electrical and Electronics Engineering from A.S.R College of Engineering, Tanuku in 2004 and the M.Sc. degree from JNTU, Hyderabad in 2007. Presently working as Associate Professor in B. V. Raju Institute of Technology, Narsapur, Telangana, India. His area of interest includes Power Electronics and Drives, Power Quality, FACTS and Artificial Neural Networks. He is currently working towards Ph.D. degree at the Department of Electrical Engineering, JNTU Hyderabad, India. He is a life member of the Indian Society for Technical Education (ISTE) and Member of the Institute of Electrical and Electronics Engineers (IEEE).

Veeramalla RAJAGOPAL was born in Kazipet, Warangal, India, in 1969. He received the AMIE (Electrical) degree from The Institution of Engineers (India), in 1999, M.Sc. degree from the Uttar Pradesh Technical University India, in 2004 and Ph.D. degree in Indian Institute of Technology (IIT) Delhi India, in 2012. Presently working as Professor in B. V. Raju Institute of Technology, Narsapur, Telangana, India. His area of interest includes power electronics and drives, renewable energy generation and applications, FACTS, and power quality. He is a life member of the Indian Society for Technical Education (ISTE) and the Institution of Engineers (India) (IE (I)) and a Member of the Institute of Electrical and Electronics Engineers (IEEE).

Askani JAYA LAXMI was born in Mahaboob Nagar District, Andhra Pradesh, in 1969. She completed her B.Sc. (EEE) from Osmania University College of Engineering, Hyderabad in 1991, M.Sc.(Power Systems) from REC Warangal, Andhra Pradesh in 1996 and completed Ph.D. (Power Quality) from Jawaharlal Nehru Technological University, Hyderabad in 2007. She has five years of Industrial experience and 14 years of teaching experience. Presently, working as Professor, Electrical & Electronics Engineering, and Coordinator, Centre for Energy Studies, JNTUH College of Engineering, Jawaharlal Nehru Technological University Hyderabad, Kukatpally, and Hyderabad. She has 45 International Journals to her credit and also has 100 International and National papers published in various conferences held at India and also abroad. Her research interests are Neural Networks, Power Systems & Power Quality. She was awarded "Best Technical Paper Award" in Electrical Engineering from Institution of Electrical Engineers in the year 2006. Dr. A. Jaya Laxmi is a Member of IEEE, Member of International Accreditation Organisation (M.I.A.O), Fellow of Institution of Electrical Engineers Calcutta (F.I.E), Life Member of System Society of India (M.S.S.I), Life Member of Indian Society of Technical Education (M.I.S.T.E), Life Member of Electronics & Telecommunication Engineering (M.I.E.T.E), Life Member of Indian Science Congress (M.I.S.C).