A New Control Strategy Based Multi Converter UPQC Using Fuzzy Logic Controller to Improve the Power Quality Issues

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Abstract. *A design of multiconverter unified power quality conditioner to improve the power quality issues is presents in this paper. Modified SRF theory and fuzzy logic controller technique are incorporated in this modelling. This newly designed controller is connected to a source in order to compensate voltage and current in the two feeders. The expanded concept of UPQC is multi converter-UPQC; this system has two series voltage source converter (VSC) and one shunt VSC connected back to back. In the proposed system, the power can be conveyed from one feeder to another in order to mitigate the voltage sag, swell, interruption and transient response of the system. The control strategies of multi converter-UPQC are designed based on the modified synchronous reference frame theory with fuzzy logic controller. The transient response of the fuzzy logic controller in dc-link voltage controller will be very fast. The relevant simulation and compensation performance analysis of multi converter-UPQC with fuzzy logic controller is performed using MATLAB/Simulink software.*

Keywords

Fuzzy logic controller, MC-UPQC, modified synchronous reference frame theory, power quality, voltage source converter.

1. Introduction

The Flexible AC Transmission System (FACTS) is generally being used for faster damping of power swing, to control the power flow and to load the transmission line within their thermal limits securely. In the distribution system the power electronic devices were used to increase the reliability and quality of the power supplied to consumers. A new technology with the application of power electronics devices in power distribution system for the benefit of consumer or a group of consumers is called "Custom Power Devices (CPD)". The use of power electronics device such as UPQC is connected combination of both in shunt and series side; to mitigate problems such as frequency of rare power interruption, over/under voltages of magnitude and duration within limits; low harmonic distortion, low phase unbalance, low voltage flicker in the supply side and frequency of the supply voltage (According to IEEE 1159-1995 standard).

A custom power device provides an integrated solution to the present problems that are faced by the utilities and power distribution. The various compensating devices are DSTATCOM, DVR and UPQC; among these the UPQC provides good solutions when compared to the other devices. Because it is a very versatile device that can inject current in shunt side and voltage in series side simultaneously in a dual control mode. Hence it can perform both the functions in load compensations. Power quality variations are classified as disturbances or steady state variations. Disturbances pertain to be abnormalities in the system voltage /currents due to a fault or some abnormal operations [1].

The Multi-Converter UPQC (MC-UPQC) system has three Voltage Source Converter (VSC's) connected to two feeder lines to compensate the voltage and current imperfection in both feeders [2]. The control parts of the shunt and series Active Power Filters (APF) are proposed based on Synchronous Reference Frame (SRF) theory with Proportional Integral (PI) controller. SRF based control for a dynamic model in three phase system under different load consideration is used to improve the Power Quality (PQ) by using multiconverter with power conditioner [3]. The Interline Unified Power Quality Conditioner (IUPQC) consists of series VSC and shunt of VSC both joined together by a common dc bus. It can also be used to demonstrate how it is connected between two indepen-

dent feeders in regulating the voltage across a sensitive load from the other feeder [4]. The Generalized Unified Power Quality Conditioner (GUPQC) is a combination of one shunt and two series VSC to compensate current imperfections in one feeder and voltage imperfection in the other two feeders [5].

In the study of reference current generation techniques using VSC based DSTATCOM for reactive power compensation, source current balancing and harmonic mitigation in delta connected for different control techniques such as Instantaneous Reactive Power (IRP), SRF and Symmetrical component (SC) theory have been used [6]. The Convertible Unified Power Quality conditioner (CUPQC) is connected to multi-bus/multifeeder distribution system to mitigate current and voltage interruptions [7]. The control strategy of the UPQC is to contribute on the flow of instantaneous active and reactive powers inside the UPQC [8]. The comparison of Unified Power Flow Controller (UPFC) and UPQC are studied and its advantages are found to be over conventional APF's [9]. A four wire capacitor midpoint shunt APF with a predictive control technique is used to mitigate the current harmonics and the neutral current. A different type of controller methods exists to improve the power quality problems based on the PI control also many theories are available [11], [12], [13], [14], [15], [16], [17], [18], [19].

In all the above mentioned techniques PI controller is used for designed UPQC. In order to regulate the DC-link capacitor voltage, a conventional PI controller is used to maintain the DC-link voltage at the reference value. The transient response of the PI controller in DC-link voltage will be very slow. To overcome this problem a better controller is proposed to improve the transient response of the dc-link voltage. The conventional UPQC is also modified; with the new control techniques based on Modified Synchronous Reference Frame theory (MSRF) to overcome the power quality problems such as voltage/current unbalance, harmonics, reactive power compensation, voltage sag, swell and interruptions.

2. Proposed System Description

The MC-UPQC is connected before the load to make load voltage and current free from any distortions. A two feeder system is designed to interconnect with MC-UPQC as shown in Fig. 1.

The reactive current drawn from the source will be in such a way that it is in-phase with the feeder voltages. The schematic structure of the proposed MC-UPQC is given in Fig. 2. In this configuration, feeder one is connected to a non-linear load and feeder two is connected to a linear load; with MC-UPQC the two feeders are connected. The MC-UPQC operation is the combination of two series voltage converter and one shunt voltage converter which are connected back-to-back with a common DC-link capacitor, by which it can be Controlled independently to compensate the power quality problems. Due to non-linear load in feeder one, system is affected with unbalanced voltage/currents, harmonic distortions in the source as well as in load sides of the both feeders.

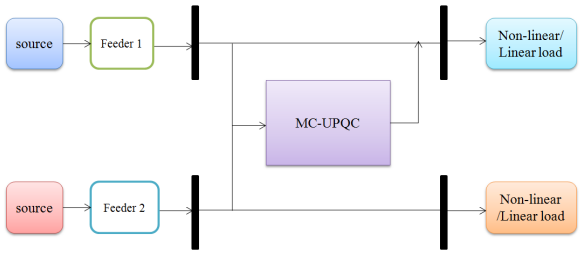

Fig. 1: Single line diagram of MC-UPQC.

As per feeder two the load is a linear load hence it has no harmonic distortion, sag, swell, interruption, voltage/current unbalance, hence it has no effect in both the feeders. The two series VSC's are connected in the series between the two feeders through a series transformer, the shunt VSC is connected to feeder one through a shunt transformer in load side. To avoid the flow of switching harmonics in MC-UPQC the power RC high pass filter with commutation reactor (L) is connected to all VSC's. To achieve this, we examine one suitable structure of the MC-UPQC with Fuzzy Logic Controller (FLC).

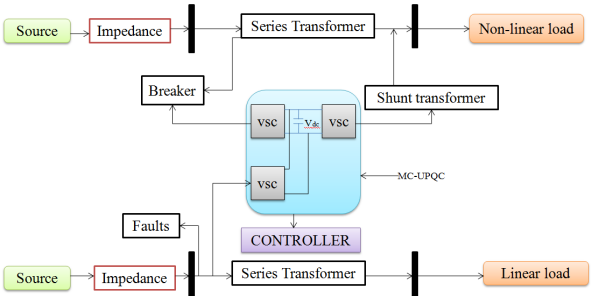

Fig. 2: Single line diagram of MC-UPQC.

3. Control Strategy for the MC-UPQC

The proposed control strategy aims to generate reference signals for both shunt and series voltage source converter of the MC-UPQC. The control technique is capable of extracting most of the load currents, source

$$\begin{bmatrix} i_{l-d} \\ i_{l-q} \\ i_{l-0} \end{bmatrix} = \begin{bmatrix} I_d \\ I_q \\ I_0 \end{bmatrix} \begin{bmatrix} i_{l-a} \\ i_{l-b} \\ i_{l-c} \end{bmatrix} \tag{1}$$

$$\begin{bmatrix} I_d \\ I_q \\ I_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \sin wt & \sin\left(wt - \frac{2\pi}{3}\right) & \sin\left(wt + \frac{2\pi}{3}\right) \\ \cos wt & \cos\left(wt - \frac{2\pi}{3}\right) & \cos\left(wt + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \tag{2}$$

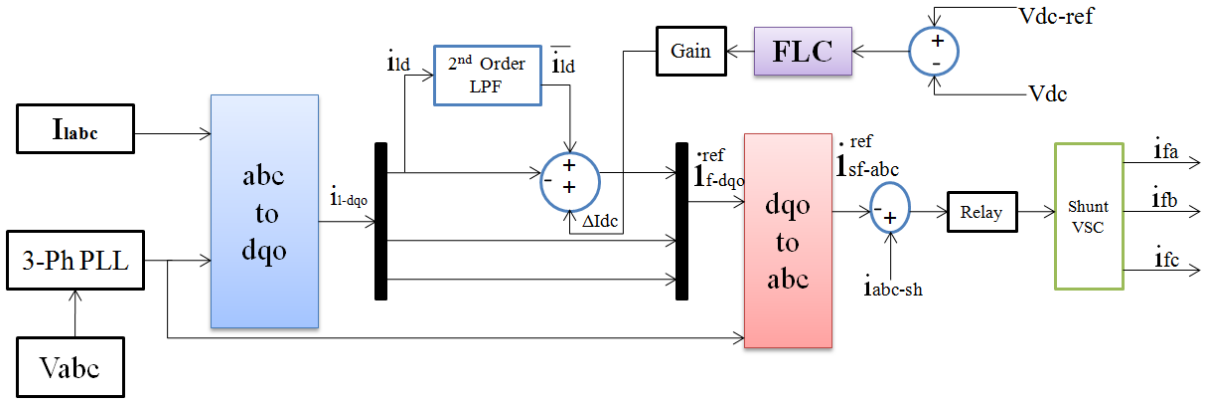

Fig. 3: SRF based control strategy of the shunt VSC.

voltage distortions, voltage sags, swell and harmonics, voltage and current unbalance, reactive and harmonic component of the both feeders.

3.1. The Control Scheme of the Shunt VSC

The control algorithm for the shunt VSC block is shown in Fig. 3. The shunt VSC used in the simulation is designed by using MSRF theory with FLC technique. When compared to the conventional method [2], the designed system of shunt VSC gives the better compensating of harmonics, reactive components of feeder one load current as well as to regulate the common DC-link capacitor voltage. When the supply voltage is got distorted, a phase-locked loop (PLL) is used to achieve synchronization with the supply voltage. The distorted supply voltage is sensed and given to PLL to generate two quadrature unit vectors, namely sine and cosine outputs from the PLL in order to compute the 120° phase displacement for each phase. The shunt VSC is based on the unit vector template, based on the concept of MSRF theory. According to this theory, the phase angle of each phase voltage and currents can be extracted as a three independent two-phase system usually given by Π/2 lead or lag. This theory can be applied for three-phase balanced system as well as unbalanced of each phase system independently.

The three phase load currents for feeder one is transformed into load synchronous reference currents using Eq. (1) and Eq. (2).

The fundamental direct axis component current is transferred into DC quantities using 2nd order low-pass-filter and it is added to the fuzzy logic output to generate a new reference shunt feeder currents in Eq. (3) and Eq. (4):

$$i_{f-d}^{ref} = \overline{i_{ld}} + \Delta I_{dc}, \tag{3}$$

$$i_{f-q}^{ref} = i_{l-q}, \tag{4}$$

$$\begin{bmatrix} i_{f-a}^{ref} \\ i_{f-b}^{ref} \\ i_{f-c}^{ref} \end{bmatrix} = \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \begin{bmatrix} i_{f-d}^{ref} \\ i_{f-q}^{ref} \\ i_{f-0}^{ref} \end{bmatrix}. \tag{5}$$

The power received from the DC-link capacitor through the series inverter and switching losses can be used to decrease the average value of DC bus voltage. All other distortions like unbalance conditions and sudden change in load current can also result in oscillations in DC bus voltage. In order to overcome the

$$\begin{bmatrix} v_{l-d} \\ v_{l-q} \\ v_{l-0} \end{bmatrix} = \begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} \begin{bmatrix} v_{l-a} \\ v_{l-b} \\ v_{l-c} \end{bmatrix} \tag{6}$$

$$\begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \sin wt & \sin\left(wt - \frac{2\pi}{3}\right) & \sin\left(wt + \frac{2\pi}{3}\right) \\ \cos wt & \cos\left(wt - \frac{2\pi}{3}\right) & \cos\left(wt + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{7}$$

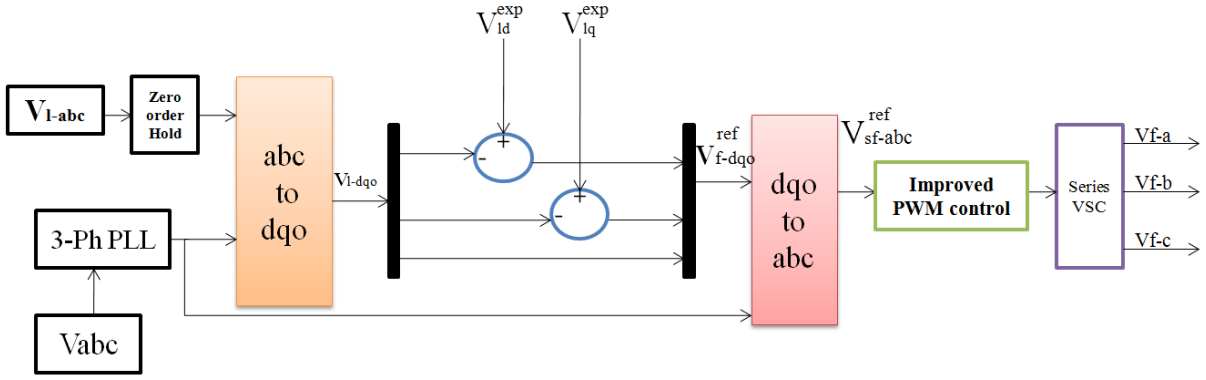

Fig. 4: SRF based control strategy of the series VSC.

error between the desired capacitor voltage and measured values, both are applied to fuzzy logic controllers. The output controlling signal is applied to the current control system of shunt VSC, which stabilizes the DC capacitor voltage by receiving required power from the source. The direct component of the feeder current is subjected to load direct components and quadrature components of the feeder current is subjected to zero. Hence, there is no harmonic current and reactive component in feeder one. The new reference shunt feeder currents in Eq. (3) and Eq. (4) are transformed back to the abc reference currents in Eq. (5).

The shunt currents are added to the abc reference frame currents and it is sensed by the relay to control the currents. The compensation currents of shunt VSC are directly given to controller part is shown in Fig. 3. In section 4 are discussed details about fuzzy logic control operation.

3.2. The Control Scheme of the Series VSC

The control algorithm for the series VSC block is shown in Fig. 4. The series VSC is proposed using MSRF theory with the improved PWM generator are proposed.

Compared to the conventional method [2], the proposed system of series VSC's gives the better compensation of voltage sag, swell and interruptions in feeder two alone, voltage distortions, harmonic distortions and load voltage unbalance in both feeders. The series VSC block is based on the unit vector template by the new MSRF theory. The distorted three-phase supply voltages were sensed by PLL to generate two quadrate unit vectors. The three phase load voltages are transformed into load synchronous reference voltages using Eq. (6), Eq. (7).

According to series control objective, even if the supply voltage is concerned the load voltage must be kept sinusoidal with constant amplitude. So, the expected load Synchronous reference *dqo* voltages are subtracted from the V_{l-dqo} in Eq. (8) and its compensation reference feeder dqo voltages are transformed back to the synchronous reference feeder voltages using Eq. (9):

$$\begin{bmatrix} v_{f-d}^{ref} \\ v_{f-q}^{ref} \\ v_{f-0}^{ref} \end{bmatrix} = \begin{bmatrix} v_{l-d} \\ v_{l-q} \\ v_{l-0} \end{bmatrix} \begin{bmatrix} v_{f-d}^{exp} \\ v_{f-q}^{exp} \\ v_{f-0}^{exp} \end{bmatrix}, \tag{8}$$

$$\begin{bmatrix} v_{sf-a}^{ref} \\ v_{sf-b}^{ref} \\ v_{sf-c}^{ref} \end{bmatrix} = \begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix}^{-1} \begin{bmatrix} v_{f-d}^{ref} \\ v_{f-q}^{ref} \\ v_{f-0}^{ref} \end{bmatrix}. \tag{9}$$

The compensation synchronous reference *abc* voltages are forwarded to the improved PWM generator.

The output of the PWM generator compensation voltage is directly given to control part of series VSC as shown in Fig. 4.

3.3. Design of New Source Controller

The design of the new source controller which gives the supply voltage to the system block diagram is shown in Fig. 5. In this controller six sine waveforms (SW) are considered in continuous mode operation. It is modified by the change of amplitude, angular frequency and phase sequence to get the discrete sine waveform. The sine wave determines the computational technique used the parameters in the two types are related Eq. (10) and Eq. (11):

$$S_p = \frac{2\Pi}{(ft + \Phi)} + B, \tag{10}$$

$$N_{os} = \frac{P \times S_p}{2\Pi}, \tag{11}$$

$$S_0 = V_{sin}.(ft + \Phi) + B, \tag{12}$$

where Sp = samples per period, f = frequency, t = time period, B = bias, Φ = phase angle, N_{os} = number of offset samples, P = phase sequence, S_0 = signal output, V = sine wave amplitude.

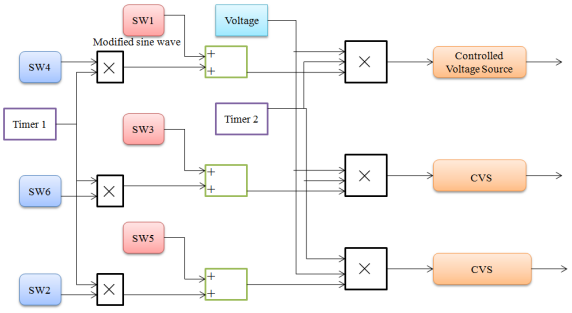

Fig. 5: Block diagram of Source controller.

Here, it is considered the bias value is zero, with phase degree of 120° phase shift. The signal output equation of the sine wave is given in Eq. (12). The modified SW1, SW3, SW5 are connected with timer 2 (t_2). Similarly the SW4, SW6, SW2 are connected with timer 1 (t_1). The SW1, SW4 are added and the output of the signals is multiplied by phase voltage and it is sensed signal to CVS. The three phase source voltage is generated by using below Eq. (13), Eq. (14) and Eq. (15).

$$S_a = V_p[SW1 + (SW4 \times t_1)] \times t_2, \tag{13}$$

$$S_b = V_p[SW3 + (SW6 \times t_1)] \times t_2, \tag{14}$$

$$S_c = V_p[SW5 + (SW2 \times t_1)] \times t_2. \tag{15}$$

Where, V_p is the phase-phase rms voltages, t_1 and t_2 are the timers to generate a signal changing at a specified time. Assume SW1, SW3, SW5 are upper switches and SW4, SW6, SW2 are lower switches. Generally, an ideal voltage source is a mathematical abstraction that simplifies the analysis of electrical circuits. If the voltage across an ideal voltage source can be specified independent voltage source. Conversely, if the voltage across an ideal voltage source is determined by some other voltage or current in a circuit then it is called a "dependent or controlled voltage Source (CVS)".

The use of controlled voltage source is converting the simulink input signal into an equivalent voltage source. The generated voltage is driven by the input signal of the block, and then it initializes the circuit with a specific AC to DC voltage [20]. To start the simulation in steady state, the block input must be connected to a signal starting as a sinusoidal or DC waveform corresponding to the initial values. The design parameters of source controller are shown in Tab. 1.

Tab. 1: Design parameters of source controller.

Parameters	Upper switches (SW1, SW3, SW5)	Lower switches (SW4, SW6, SW2)
Amplitude	0.22	1
Bias	0	0
Φ [deg]	120°	120°
ω [rad/s]	$2 \cdot \Pi \cdot 50 \cdot 7$	$2 \cdot \Pi \cdot 50$
Sample time	$50e^{-6}$	$50e^{-6}$

4. Fuzzy Logic Controller

Fuzzy logic control (FLC) system is composed of the following four principal components:

- fuzzification,
- knowledge base,
- inference engine or decision making logic,
- de-fuzzification.

The output from the database and the rules of the knowledge base which were used to get the inference relation B mentioned in Eq. (16). The input and output variables of the controlled system or data bus contain a description of fuzzy sets. The paper deals with fuzzy memberships that are designed based on the Eq. (16).

$$B^{(p)} = IF\ X_1\ is\ F_1\ AND\ X_2\ is\ F_2 \ldots X_n\ is\ F_n \text{ then } Y\ is\ C^{(p)}, \tag{16}$$

where $X_1, X_2 ... X_n$ is the input variables vector, Y is the output or control variable, n is the nomber of

fuzzy variables (N=5), $F_1, F_2 ... F_n$ is the fuzzy sets, $P = 1, 2, 3 ... N$, N is the number of rules (N=5).

From the given rule base, the fuzzy controller has to compute necessary specific input signal conditions that can determine its effective control action.

To design an FLC, the plant control is inferred from the two input state variables, namely error DC capacitor voltage (V_{dc}) and change in reference DC capacitor voltage error (ΔV_{dc}) in Eq. (17):

$$v_{e\ fuzzy} = v_{dc} - v_{dc}^{ref}. \tag{17}$$

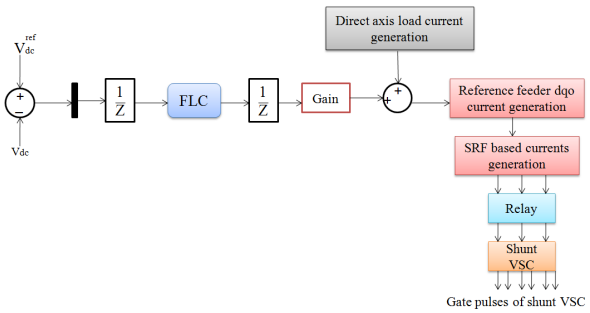

Fig. 6: Proposed structure of a complete Fuzzy logic controller.

The proposed structure of a complete FLC is given in Fig. 6. The Fuzzy control rules are designed for a fuzzy set of the control input in each combination of fuzzy sets for V_{dc} and ΔV_{dc} through which a very small amount of real loss is required for voltage regulation taken as the output from the FLC. The input and output variables are converted into linguistic variables.

The direct axis load current is added to the fuzzy logic output and it is forwarded to reference feeder dqo current. The MSRF based currents are directly given to relay and it is senses a control signal to shunt VSC control circuit.

Instead of using conventional (PI) controller mentioned in references a FLC is being used for its transient response to make MC-UPQC very fast in reducing the total harmonic distortions on the source and load side voltages as well as currents on both the feeders. Here five labels of fuzzy subsets; negative large (NL), negative medium (NM), zero (ZR), positive medium (PM), positive large (PL). The control rule base table is shown in Tab. 2. In which the row and column represent the error and its changes respectively.

Tab. 2: Rule based for Voltage control.

		INPUT 2 [ΔV_{dc}]				
		NL	NM	ZR	PM	PL
INPUT 1 [V_{dc}]	NL	NL	NL	NM	NM	ZR
	NM	NL	NM	NM	ZR	PM
	ZR	NM	NM	ZR	PM	PM
	PM	NM	ZR	PM	PM	PL
	PL	ZR	PM	PM	PL	PL

5. Simulation Results and Discussion

In order to certify the control strategy as discussed above, the MATLAB simulation based proposed system as described in Fig. 2, is compared without and with MC-UPQC controller, with (PI) controller [2]. The proposed control system gives better simulation results as expected. The same model is re-defined with some modifications and also incorporated with FLC is realized using the MATLAB/Simulink software environment as shown in Fig. 7. The performance of the MC-UPQC along with FLC is connected with two feeder system to mitigate the voltage sag swell and interruptions. The load and source voltage unbalance are effectively reduced. Reactive power compensation also achieved with the help of series compensation and the THD of load current is reduced. The proposed control strategies for the series and shunt VSC's with FLC are discussed in below. The simulation circuit diagram for MSRF based shunt and series controller is shown in Fig. 8. Design of new source controller simulation circuit diagram is shown in Fig. 9. The controller parts are discussed in section 3.

5.1. Performance of the MC-UPQC when Connected to Feeder One

The performance of the MC-UPQC which is connected to feeder one with proposed control techniques simulation results is shown in Fig. 10, Fig. 11, Fig. 12 and Fig. 13.

The MC-UPQC is turned on at the time $t = 0.02$ s. The feeder one bus voltage has voltage sag between 0.1 to 0.2 sec and voltage swell between 0.2 to 0.3 sec. This voltage contains 24.9 % of sag and 119.9 % of swell. To compensate this voltage sag, swell using MSRF based series and shunt VSC controller with FLC is presented.

THD is reduced in bus 1 voltage from 22.01 % to 21.98 % and series compensation voltage from 65.91 % to 65.80 % simultaneously load 1 voltage from 38.90 % to 24.75 %. The simulation results and harmonic spectrum of bus 1 voltage, series compensation voltage and load 1 voltage in feeder one are shown in Fig. 10, Fig. 11 respectively. The feeder one current, shunt current, non-linear current, DC-capacitor voltages in feeder one simulation results are shown in Fig. 12. The THD is reduced in feeder one current from 2.73 % to 2.45 % and shunt filter current from 15.92 % to 13.96 % simultaneously non-linear current from 13.61 % to 12.07 %. The harmonic spectrum of feeder one, shunt filter, non-linear currents in feeder one is shown in Fig. 13. These currents are improving very well when compared to the

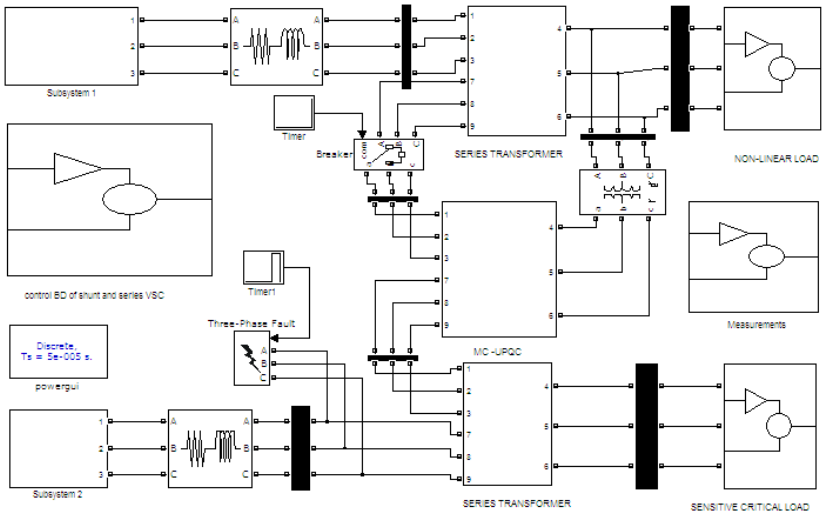

Fig. 7: Simulation circuit diagram of Multi Converter-UPQC is connected in a distribution system.

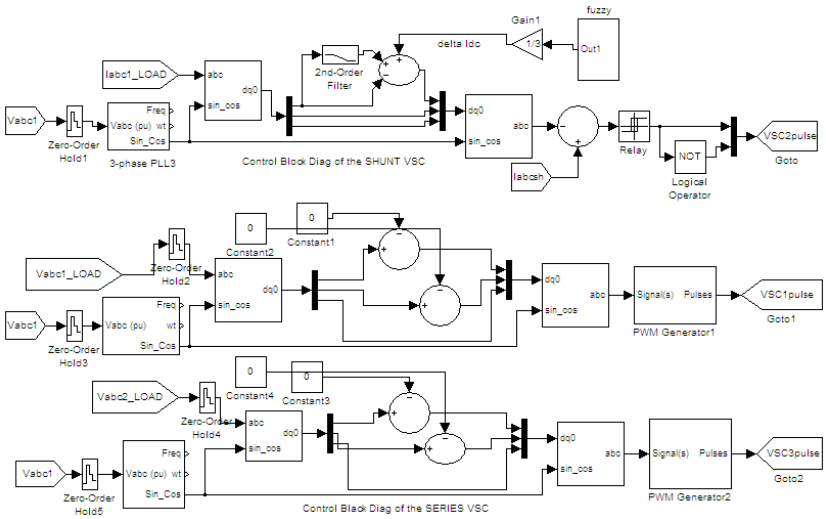

Fig. 8: Simulation control block diagram for MSRF based Shunt VSC and Series VSC controller.

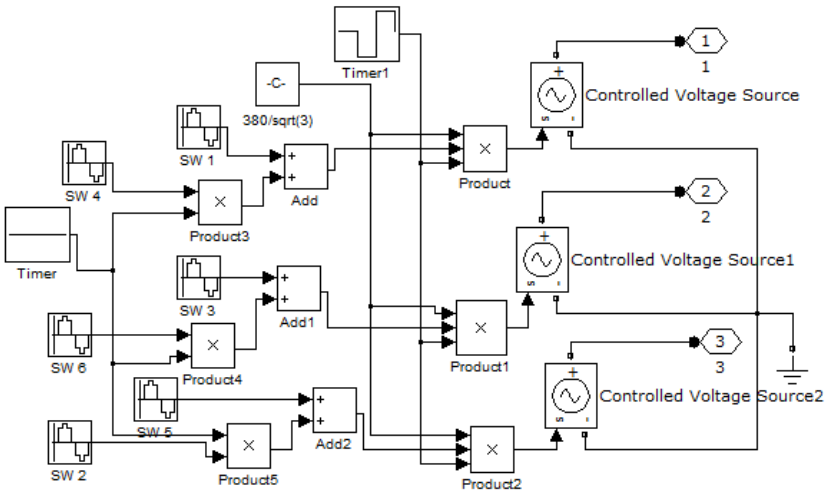

Fig. 9: Simulation circuit diagram of new source controller.

conventional system during the power quality problems in between 0.1 to 0.3 s.

5.2. Performance of the MC-UPQC when Connected to Feeder 2

The performance of the MC-UPQC connected to feeder two with proposed control techniques simulation results are shown in Fig. 14, Fig. 15, Fig. 16, Fig. 17 and Fig. 18. At the same time, the feeder two bus voltage having voltage sag between 0.15 to 0.25 s duration equal to 34.09 % is compensated using same proposed control system itself.

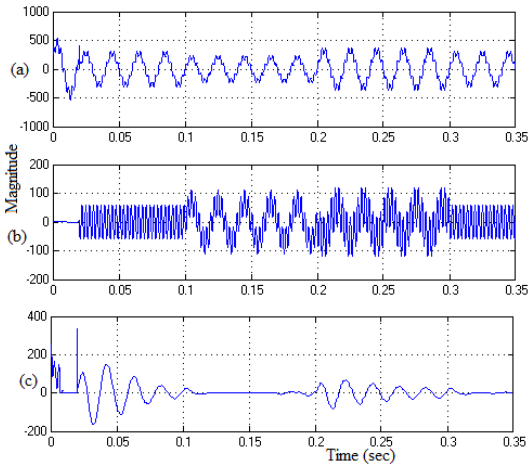

Fig. 10: Simulation results of (a) BUS 1, (b) series compensation, and (c) load 1 voltage in Feeder 1.

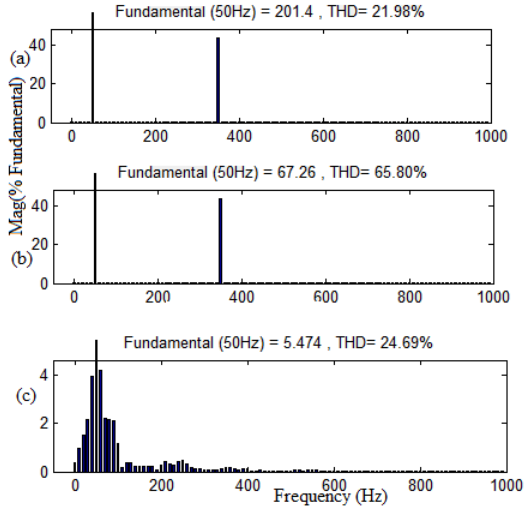

Fig. 11: Harmonic spectra of Harmonic spectrum of (a) Bus 1, (b) series compensation and (c) load 1 voltage in feeder 1.

Bus 2 having a voltage swell between 0.25 to 0.3 sec duration equal to 130 %, THD was reduced in bus 2

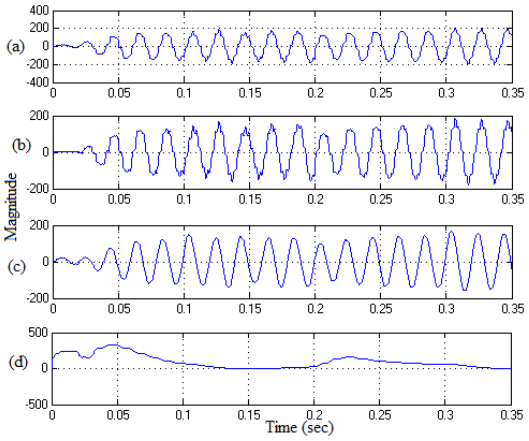

Fig. 12: Simulation results of (a) non-linear (b) shunt filter (c) feeder 1 currents and (d) DC capacitor voltage.

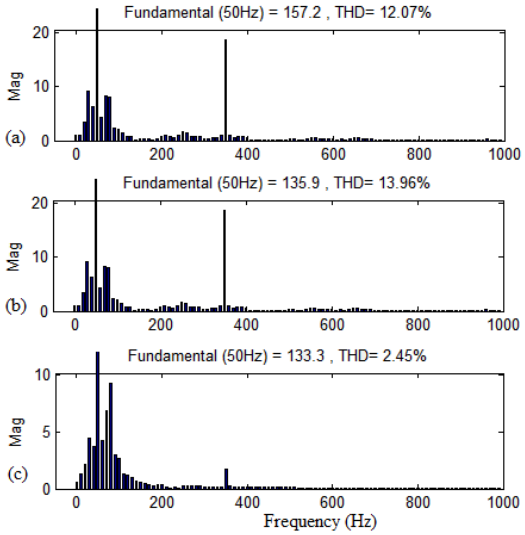

Fig. 13: Harmonic spectrum of (a) non-linear (b) shunt filter and (c) feeder 1 currents.

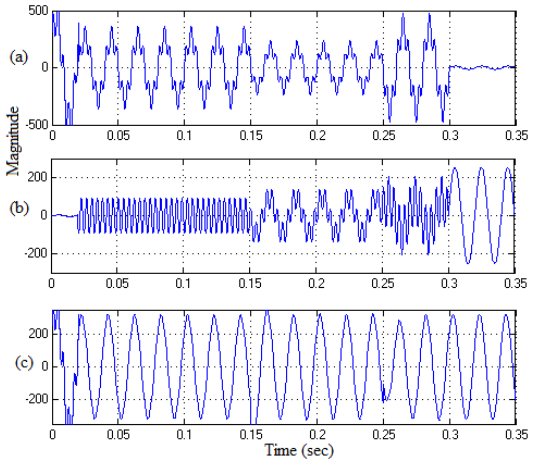

Fig. 14: Simulation results of bus 2, series compensation, load 2 voltages in feeder 2.

voltage from 34.97 % to 34.96 % and series compensa-

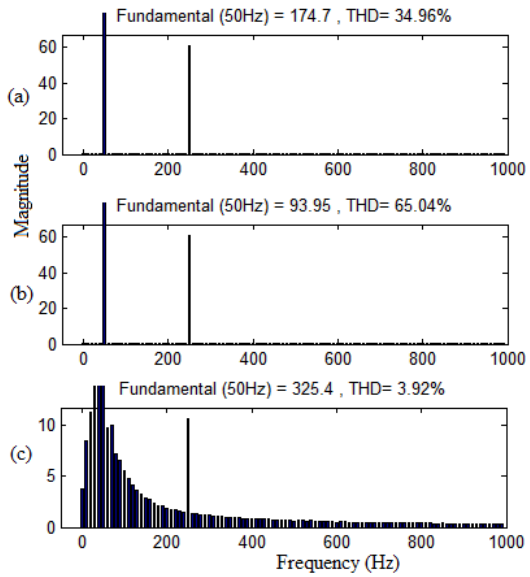

Fig. 15: : Harmonic spectra of (a) bus 2, (b) series compensation and (c) load 2 voltages in feeder 2.

tion voltage from 64.92 % to 65.04 % along with load 2 voltage from 4.30 % to 3.92 %.

The simulation results and harmonic spectrum of bus 2, series compensation and load voltages are shown in Fig. 14, Fig. 15 respectively. If any type of faults occurred in feeder two, the voltage across the linear load will be effected with sag, swell and interruptions.

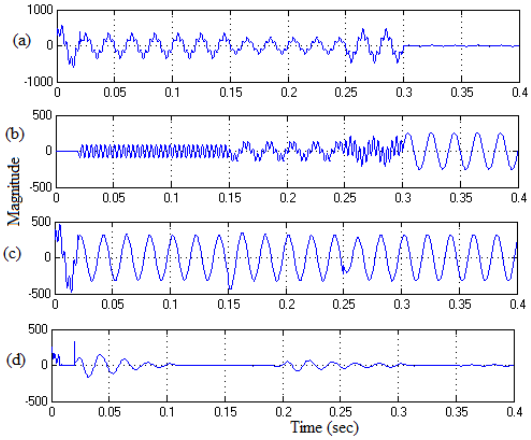

Fig. 16: Simulation results of Feeder 2 (a) bus 2, (b) series compensation, (c) load 1 and (d) load 2 voltages during upstream fault.

In order to compensate above problems a shunt VSC is used. In this paper, the system is tested with different types of faults like L-G, L-L and L-L-G faults. The L-L-L-G fault is applied to feeder two between the 0.3 to 0.4 s duration. It is observed that the bus 2 voltage is affected between 0.15 to 0.25 s duration with sag, 0.25 to 0.3 s duration with swell and 0.3 to 0.4 s duration momentary interruptions.

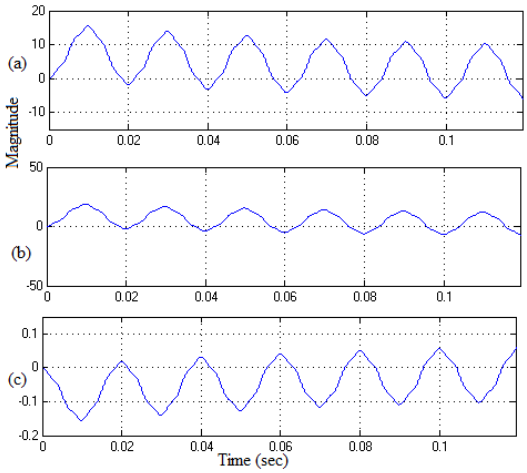

Fig. 17: Simulation results of (a) non-linear, (b) feeder 2 and (c) shunt filter current in feeder 2.

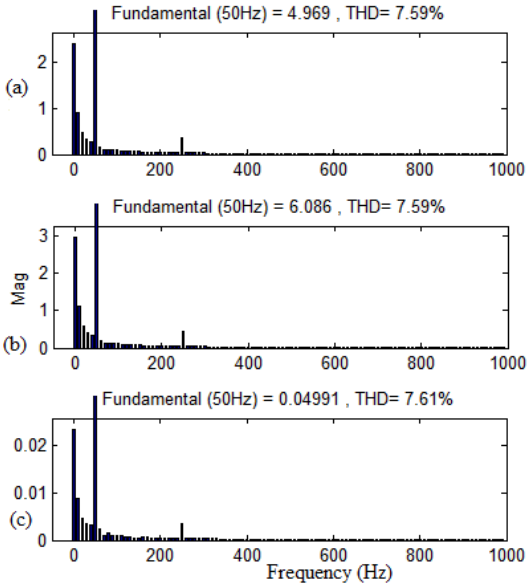

Fig. 18: Harmonic spectrum of (a) non-linear, (b) shunt filter, and (c) feeder 2 current in feeder 2.

The bus 2, series compensation, loads 1 and 2 voltages during the upstream fault conditions simulation results were shown in Fig. 16. The non-linear, feeder two and shunt currents in feeder two simulation results are also shown in Fig. 17. It is founded that THD are reduced in feeder two current from 8.92 % to 7.61 % and shunt filter current from 8.00 % to 7.59 % simultaneously non-linear currents from 8.00 % to 7.59 %. The harmonic spectrum of nonlinear, shunt filter and feeder two currents were shown in Fig. 18.

During the 0.3 to 0.4 sec, the bus 2 voltage has interruption up to 4.2 %. The above all results are compared with the conventional and proposed control system.

THD results were shown in Tab. 3, the voltage sags, swell, interruption is calculated according to IEEE

Tab. 3: % THD Results: Comparison between conventional [1] and proposed system.

System voltage/current	Without MC-UPQC	Conventional [1]	Proposed system
Bus 1 voltage(Ut1)	21.92	22.01	21.98
Compensation voltage	21.92	65.91	65.80
Load 1 voltage	21.95	38.90	24.75
Feeder 1 current	15.64	2.73	2.45
Shunt filter current	31.05	15.92	19.96
Non-linear current	15.64	13.61	12.07
Bus 2 voltage	35.08	34.97	34.96
Compensation voltage	14.11	64.92	65.04
Load 2 voltage	46.49	4.30	3.92
Feder 2 current	9.70	8.92	7.61
Shunt filter current	Undefined	8.00	7.59
Non-linear current	9.70	8.00	7.59

Tab. 4: % Results of Sag, Swell, Interruption According to IEEE 1159-1995 Std.

PQ issues [%]	Without MC-UPQC		Conventional [1]		Proposed system	
	Bus1	Bus2	Bus1	Bus2	Bus1	Bus2
Sag	25.01	35.01	25	35	24.9	34.09
Swell	119.96	130.5	120	130	119.9	130
Interruption		9.3		5		4.2

Tab. 5: % Results of Active (P), Reactive power (Q) on load and source side.

Active/reactive power	Without MC-UPQC		Conventional [1]		Proposed system	
	Load	Source	Load	Source	Load	Source
P [W]	13.82	1.745	466.6	45.23	1479	53.42
Q [var]	13.58	13.58	1170	-4.827	1792	130

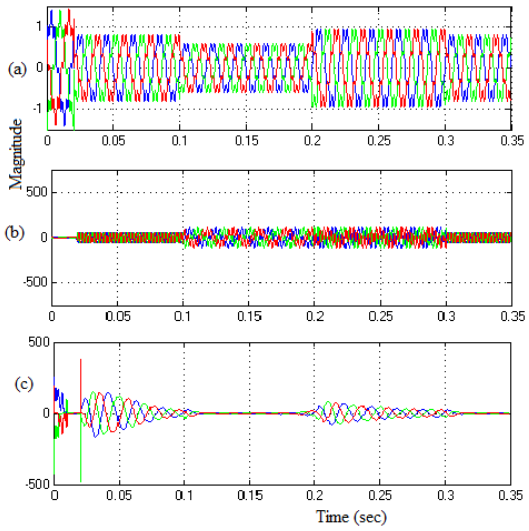

Fig. 19: Simulation results of the (a) bus1, (b) series compensation and (c) feeder 1 voltage in feeder 1 under unbalance source voltage.

1159-1995 standards as shown in Tab. 4. The active, reactive powers are calculated for both load and source side as given in Tab. 5. The simulation results for voltage at bus1, series compensated voltage and load voltage at feeder one are shown in Fig. 19. During the load changes, at the time $t = 0.5$ the load 1 voltage is doubled and it is reduced to half, reaming load is unchanged and DC bus voltage, non-linear current is compensated.

6. Conclusion

With the help of proposed MC-UPQC system the voltage /current harmonics, reactive power compensation was performed successfully. Additionally the voltage regulation was also done by protecting the loads against any distortions, sag, swell, and interruptions. By using FLC with MC-UPQC DC-link voltage controller it is observed that transient response is attained very fast. The proposed novel control strategy for a three phase three wire system utilizing with MC-UPQC is validated and compared with conventional controller.

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